AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A flash memory cell comprising:

a substrate comprising a source and a drain;

a silicon dioxide layer adjoining said substrate;

~~a polysilicon floating gate;~~

a dielectric layer ~~sandwiched between and~~ adjoining ~~both~~ said silicon dioxide layer ~~and said floating gate~~, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide;

a polysilicon floating gate adjoining said dielectric layer;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer, wherein said substrate, said silicon dioxide layer, said dielectric layer, said floating gate, said ONO layer and said control gate are arranged in a laminate structure, wherein said silicon dioxide layer is sandwiched between said substrate and said dielectric layer, wherein said dielectric layer is sandwiched between said silicon dioxide layer and said floating gate, and wherein said ONO layer is sandwiched between said floating gate and said control gate.

2-7. (Canceled).

8. (Previously Presented) The flash memory cell of Claim 1 wherein said dielectric layer comprises a composite of said metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

9. (Canceled).

10. (Currently Amended) A flash memory array comprising memory cells, wherein a memory cell comprises:

a substrate comprising a source and a drain;

~~a first layer comprising a silicon material;~~

a tunnel oxide layer ~~sandwiched between and~~ adjoining ~~both~~ said substrate ~~and said first layer~~, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide;

a first layer comprising a silicon material;

a polysilicon floating gate adjoining said first layer;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer, wherein said substrate, said tunnel oxide layer, said first layer, said floating gate, said ONO layer and said control gate are arranged in a laminate structure, wherein said tunnel oxide layer is sandwiched between said substrate and said first layer, wherein said first layer is sandwiched between said tunnel oxide layer and said floating gate, and wherein said ONO layer is sandwiched between said floating gate and said control gate.

11. (Canceled).

12. (Previously Presented) The flash memory array of Claim 10 wherein said silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

13-20. (Canceled).

21. (Currently Amended) A flash memory cell comprising:

a substrate comprising a source and a drain;

a first layer comprising a first silicon material and adjoining said substrate;

~~a second layer comprising a second silicon material;~~

a dielectric layer ~~sandwiched between and~~ adjoining ~~both~~ said first layer ~~and said second layer~~, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide, wherein said dielectric material comprises a metal oxide;

a second layer comprising a second silicon material and adjoining said dielectric layer;

a polysilicon floating gate adjoining said second layer;

an oxide-nitride-oxide (ONO) layer adjoining said floating gate; and

a control gate adjoining said ONO layer, wherein said substrate, said first layer, said dielectric layer, said second layer, said floating gate, said ONO layer and said control gate are arranged in a laminate structure, wherein said first layer is sandwiched between said substrate and said dielectric layer, wherein said dielectric layer is sandwiched between said first layer and said second layer, wherein said second layer is sandwiched between said dielectric layer and said floating gate, and wherein said ONO layer is sandwiched between said floating gate and said control gate.

22. (Original) The flash memory cell of Claim 21 wherein said first silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

23. (Original) The flash memory cell of Claim 21 wherein said second silicon material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.

24. (Canceled).

25. (Previously Presented) The flash memory cell of Claim 21 wherein said dielectric layer comprises a composite of said metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate.